Advanced PCB Partitioning Techniques

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Examples: Purposes of Partitioning

→ Separation of High-Amplitude from Low-Amplitude
(e.g. “sensitive” signals or circuit regions) for optimal functionality

→ Containment of specifically unique Spectral Regions

→ Protection of analogue circuits from digital spectra intrusion
(S/N Ratios)

→ Exclusion of EMI Emission from interface – interconnecting cables

→ Rejection of extraneously applied fields or currents
(susceptibility-immunity factors) from functional intrusion

Partitioning Initially Requires A Recognition Plan

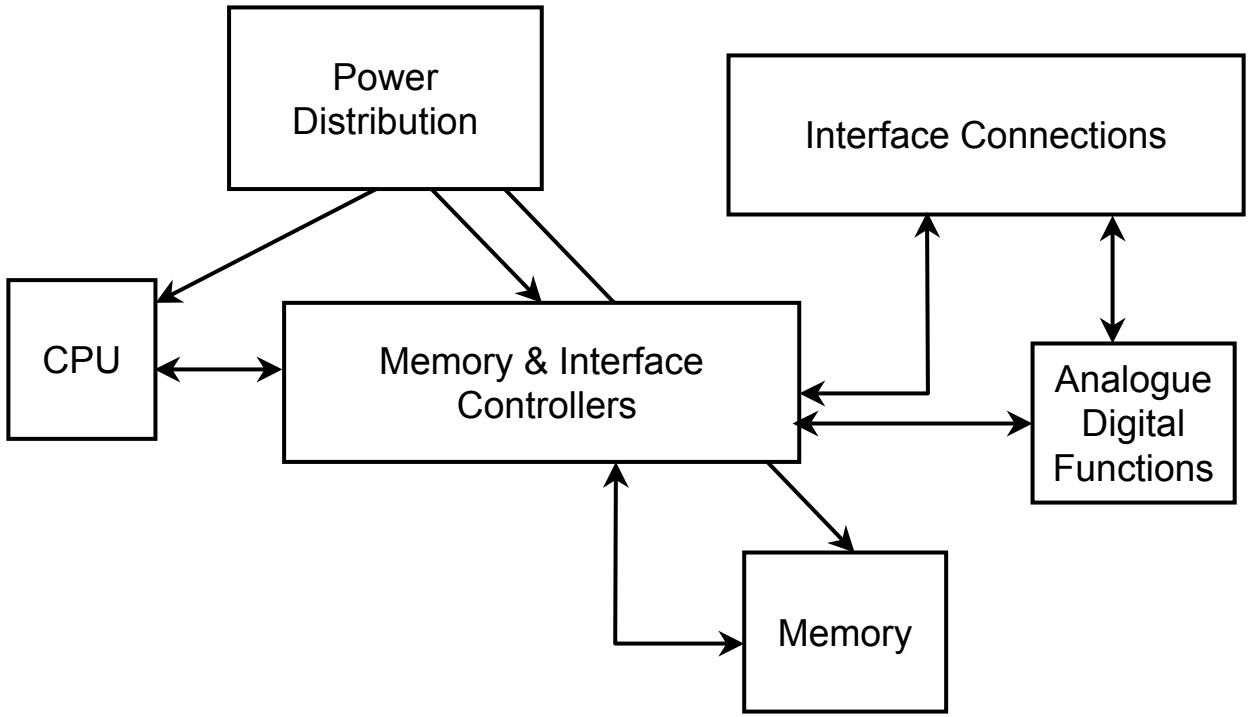
→ Recognition plan is a subset part of the system-product "Common-mode Architecture"

→ "Common-mode Architecture" is a derivative of the system-product electrical / functional block architecture

→ System-product functionality is identified initially in "block" structures

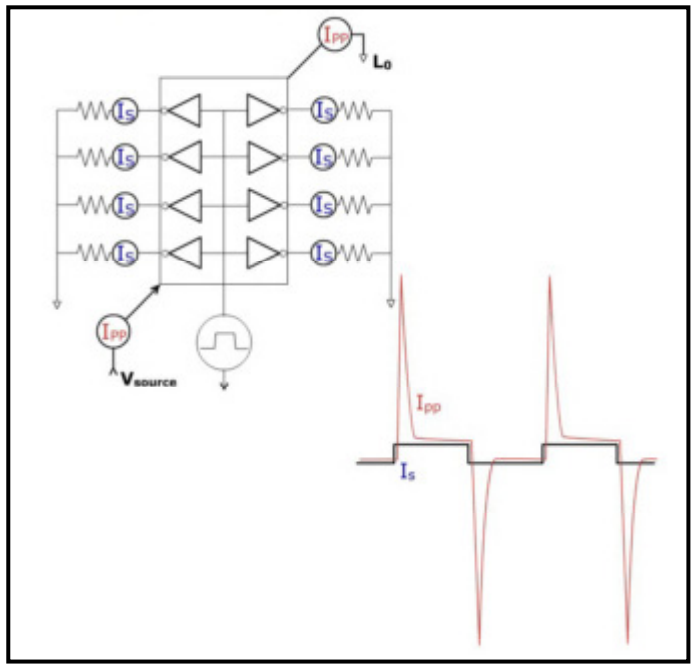
→ "Block" structures set the pattern approach initially for X-Y Axes topology, followed by Z-Axis implementations.

Electrical “Block” Architecture Initiates Process

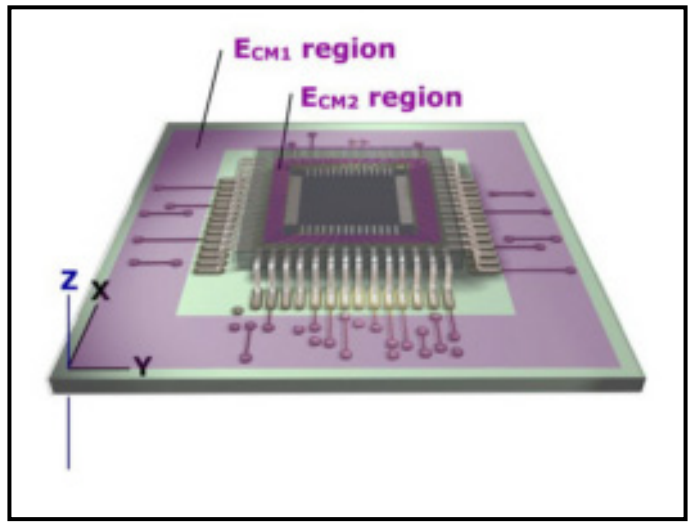


Task: Identification of “Threat Sources” and “Victim Receivers”
GOAL: EMC (Self-compatibility)

Inspection of “Threat” Sources: X-Y Axes



Peak-Current Cross-Conduction Surges With Circuit Devices……..



……Excites Common-mode Fields and Loss Potentials From Patterned Layout Inductance Surrounding Devices

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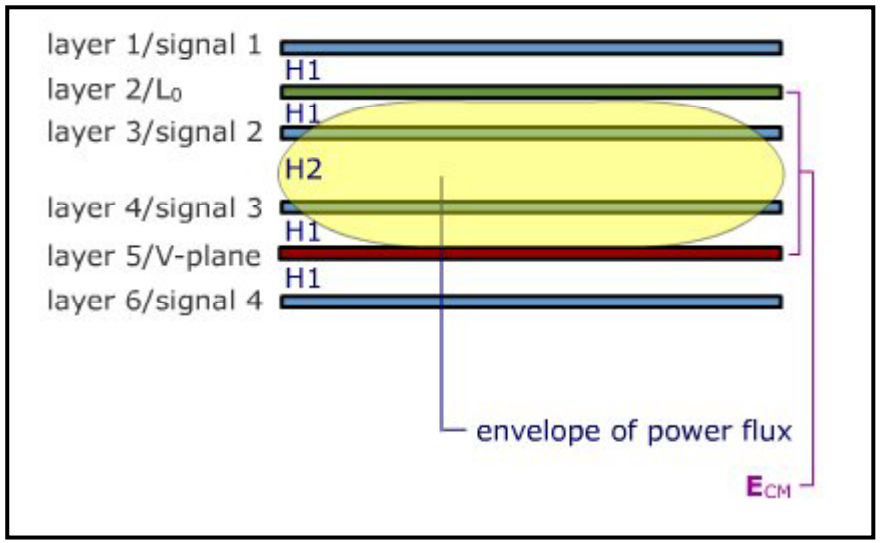
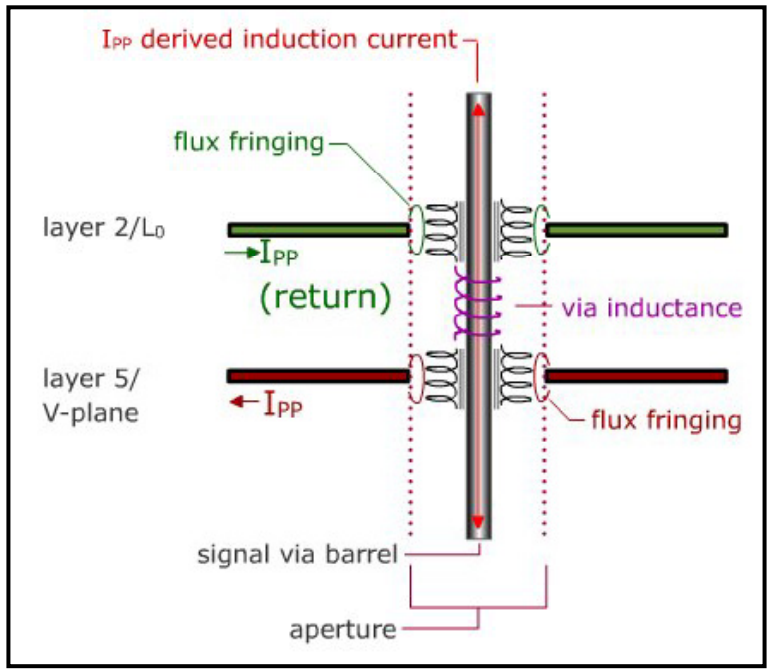
Inspection of "Threat" Sources: Z-Axis – Within Circuit Board



Inefficient Flux Cancellation Through "Stack-up, Implies Increased Common-mode Potentials, and……..



……May Degrade Signal Integrity (S/N Ratios) By POWER Flux (Current) Induction Into Z-Axis Signal Routing

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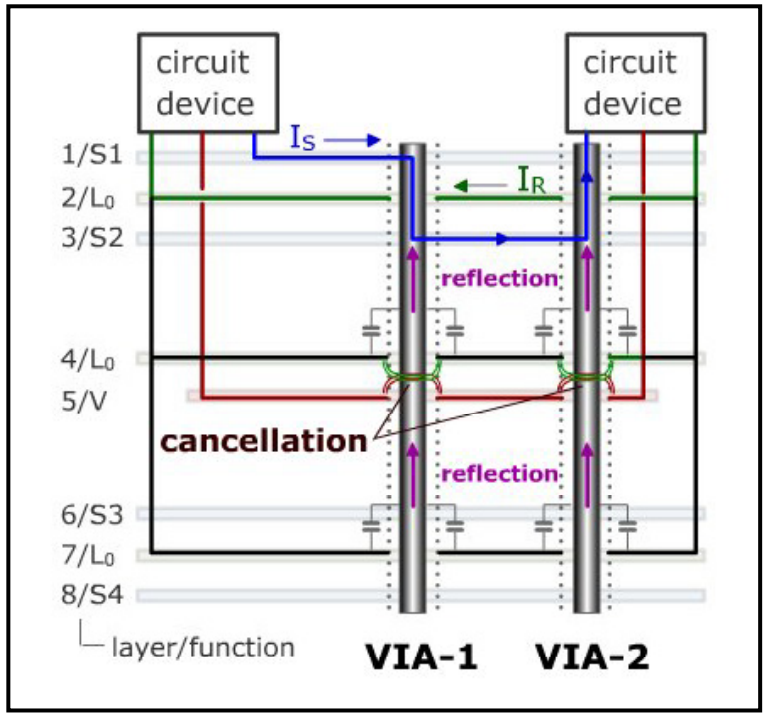
Efficient Flux Cancellation in Z-Axis – Within Circuit Board



→ **Power Impedance Is Dynamically Reduced.**
→ **Common-mode Potentials Reduced Proportionately**
→ **Power Flux Cancels in Small Loop Formations.**
→ **Signal Integrity is Defended.**

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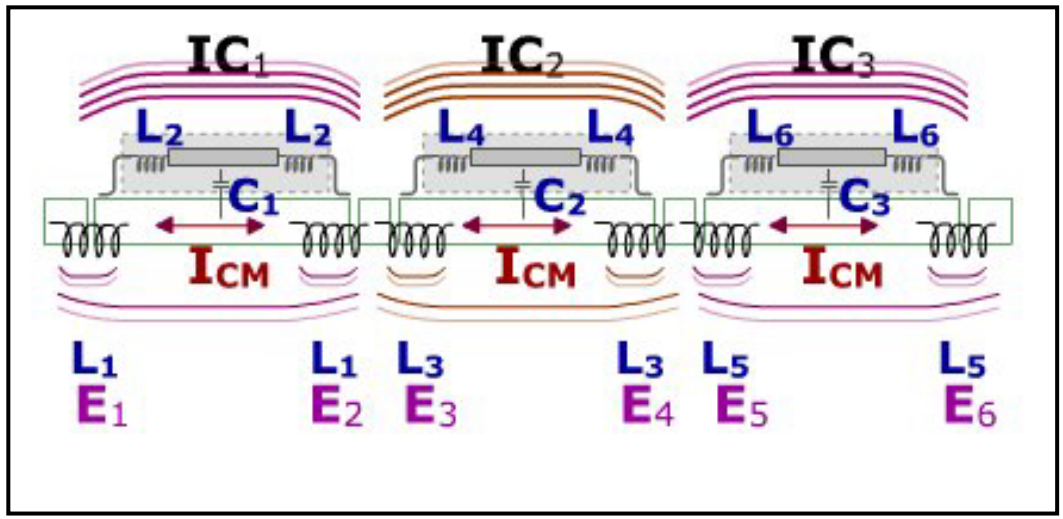
Examination of “Common-Mode Fields” From Excitation Of Patterned Layout Inductance – 3 Axes



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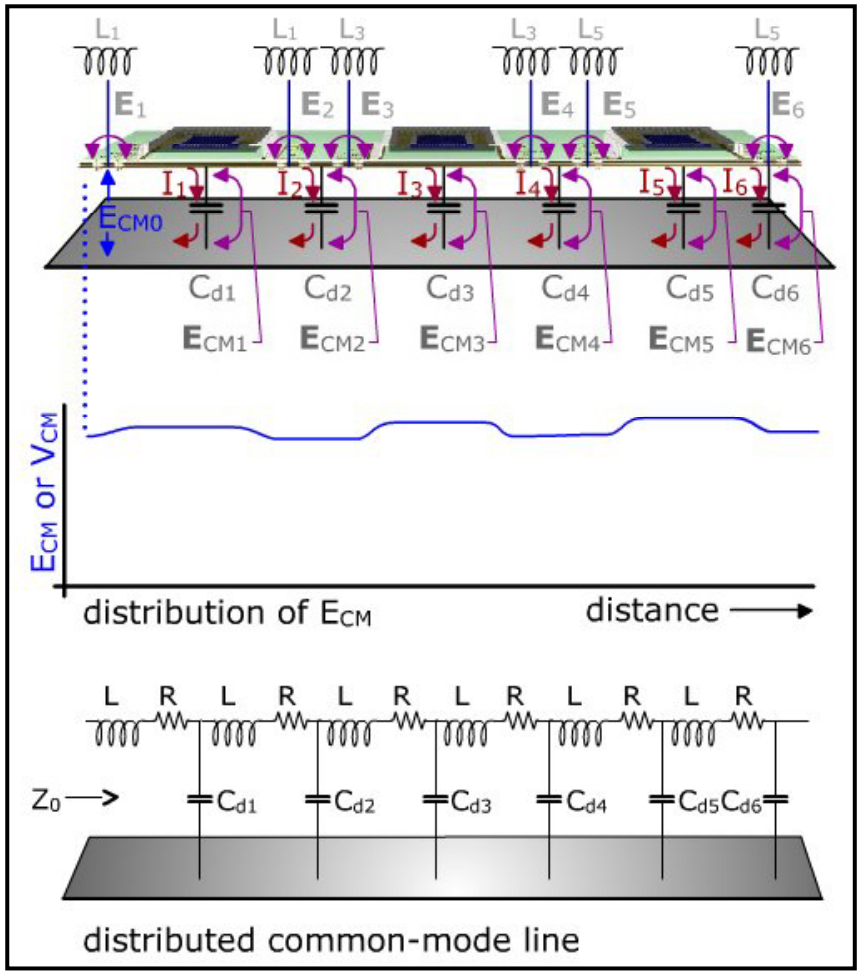
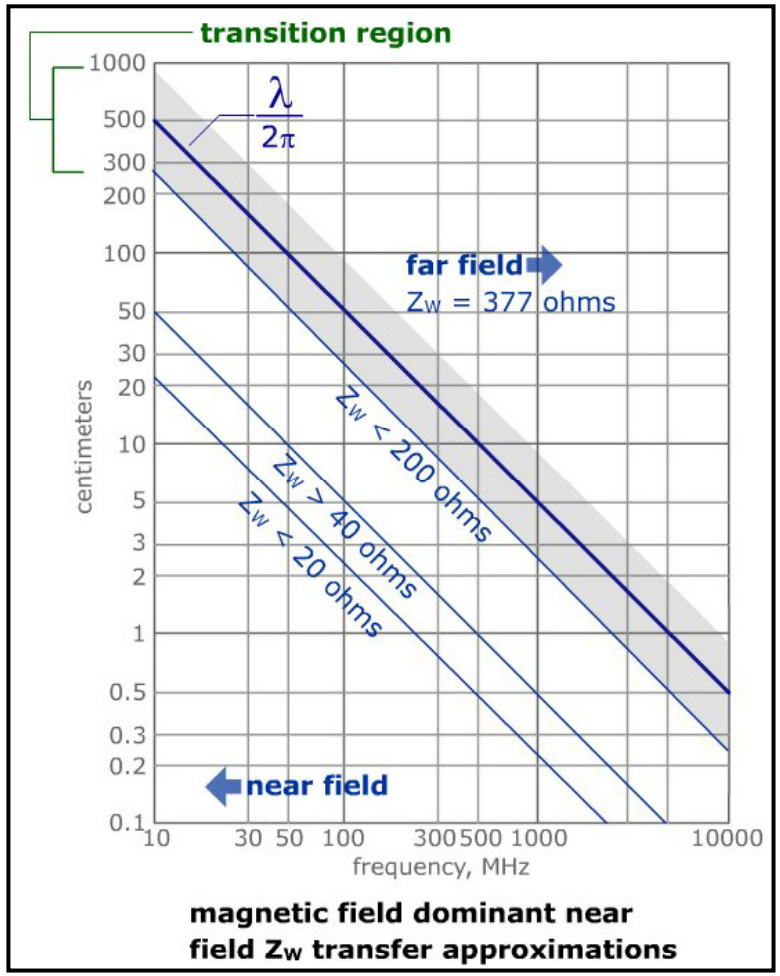
Examination of Common-Mode Field Transfers to Conductive Chassis Structures





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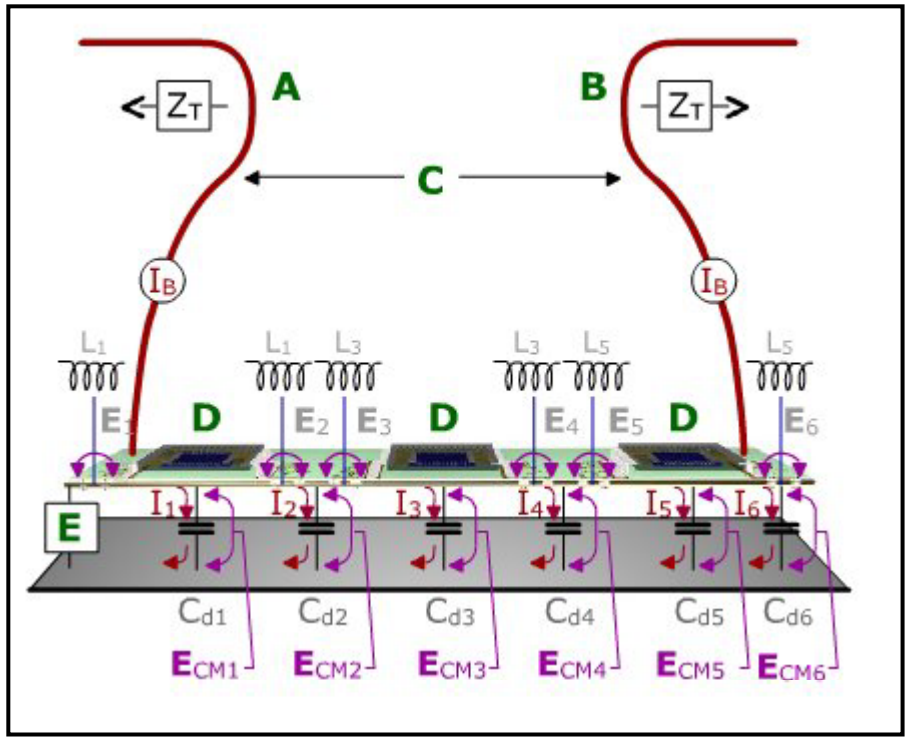
Implications of Common-Mode Transfers & Excitations in 3 Axes (Multiple Antenna Structures)



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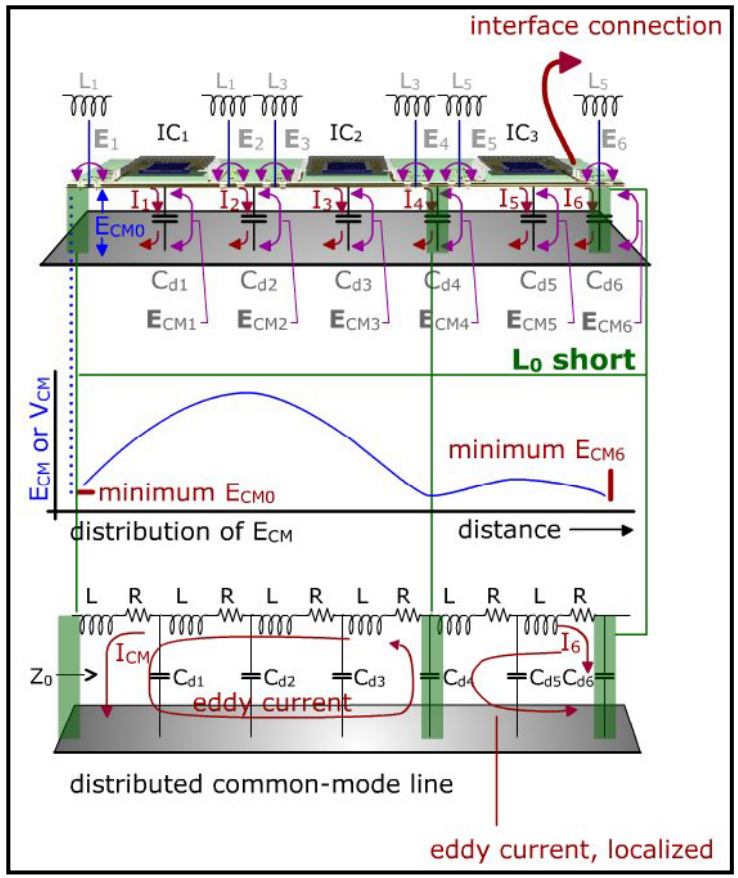
Partitioning In the Z-Axis Can Defend S/N Ratios and EMC



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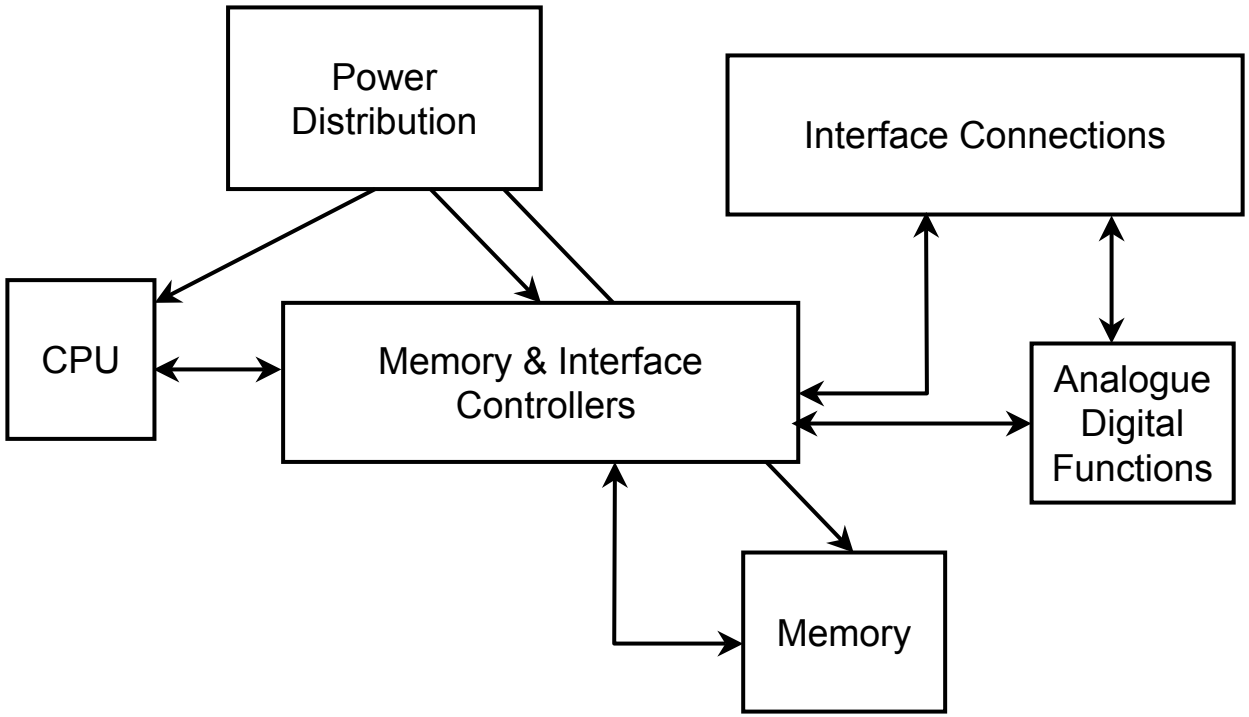
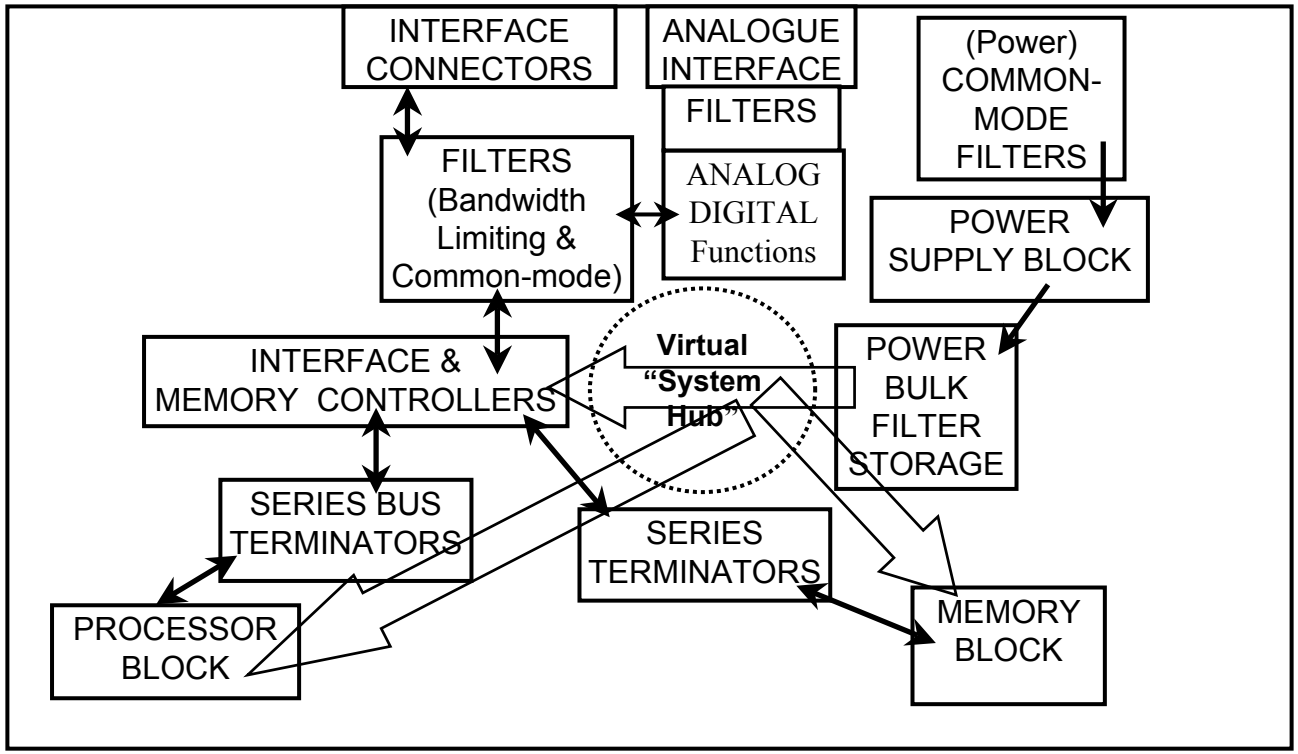
REVIEW of
Electrical “Block” Architecture

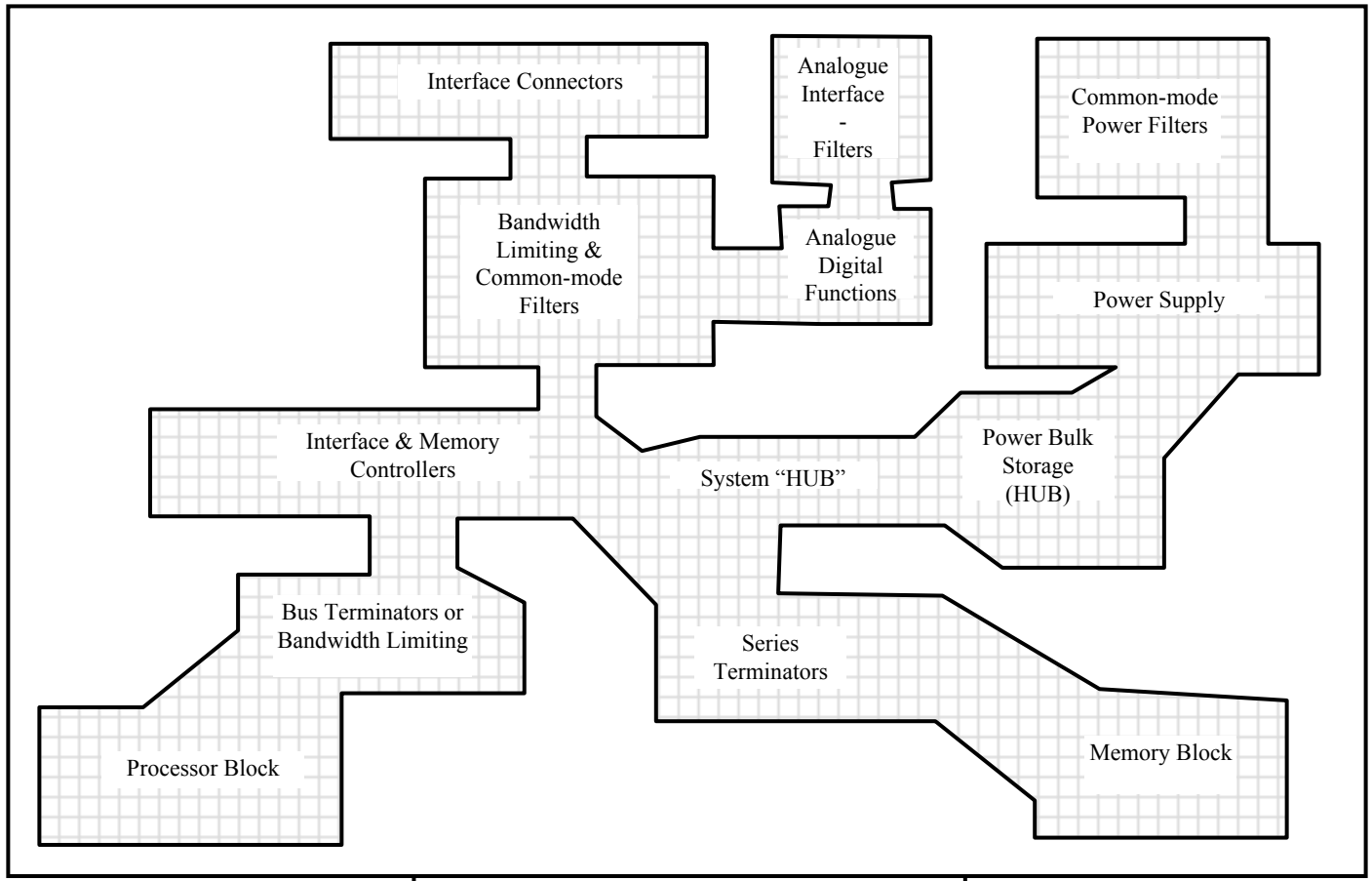


Implied Common-mode Architecture Derivative of Electrical "Block" Diagram



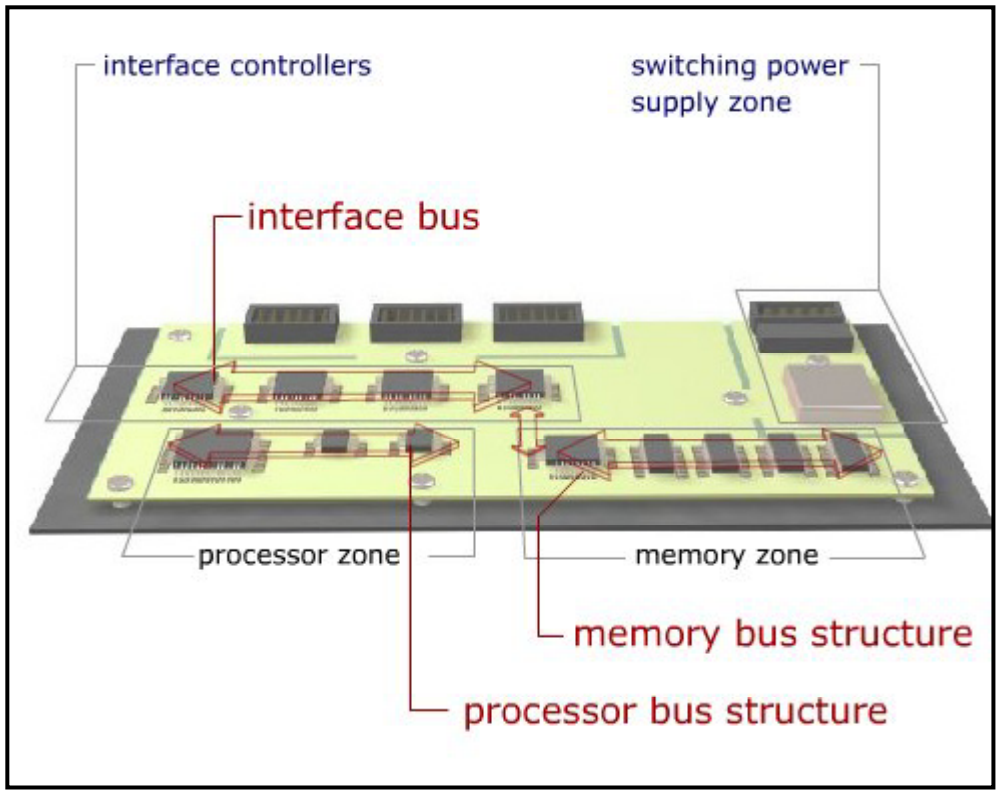
"MAP" of Architectural Topology With Function and HUB, Initially Limited to X-Y Axes

Resultant Architectural Routing Plan



Preliminary Routing "Plan" Formation

Implied Topology of Circuit Board With Chassis Plane



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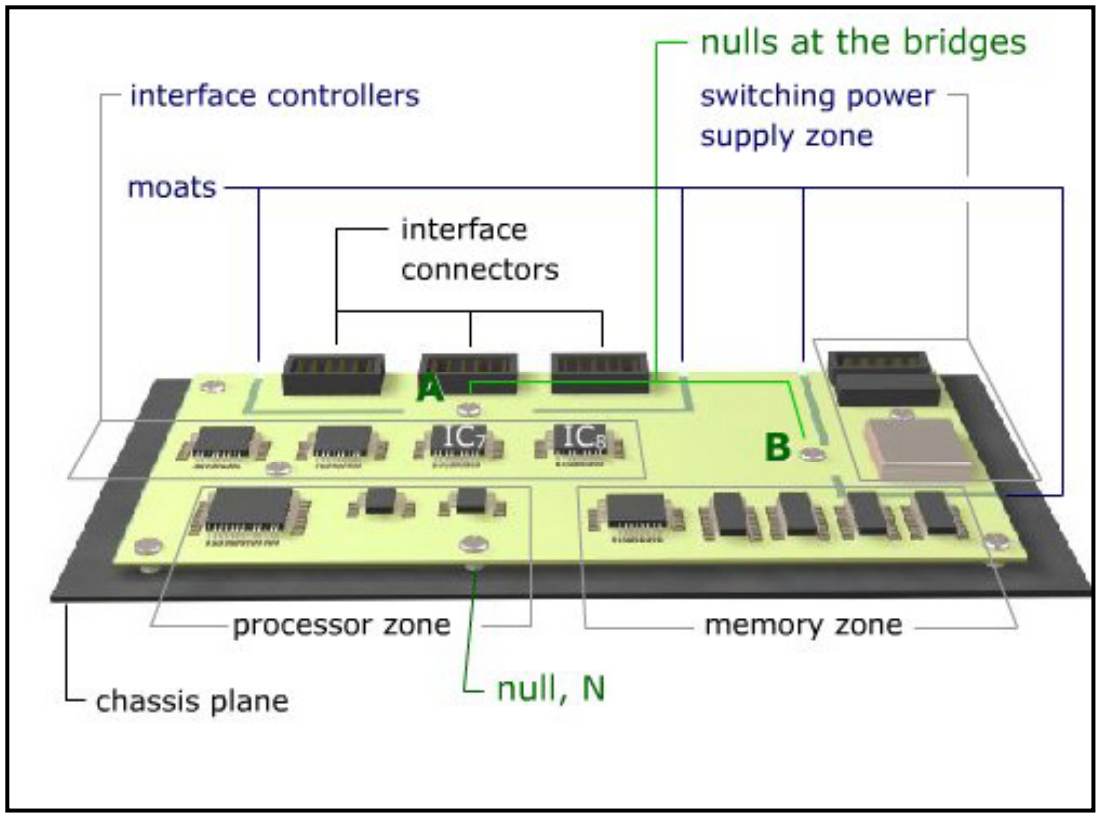
Implied Topology of Circuit Board With NULLS to Chassis Plane



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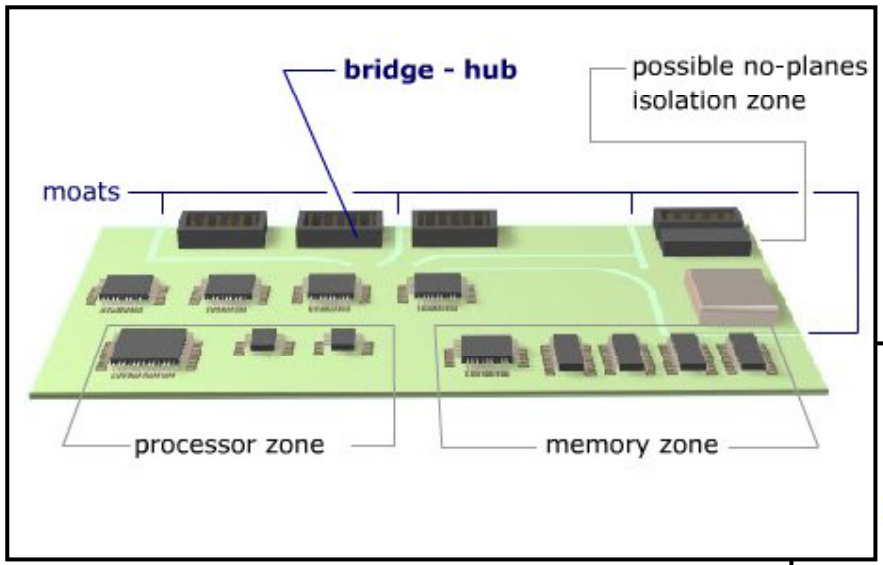
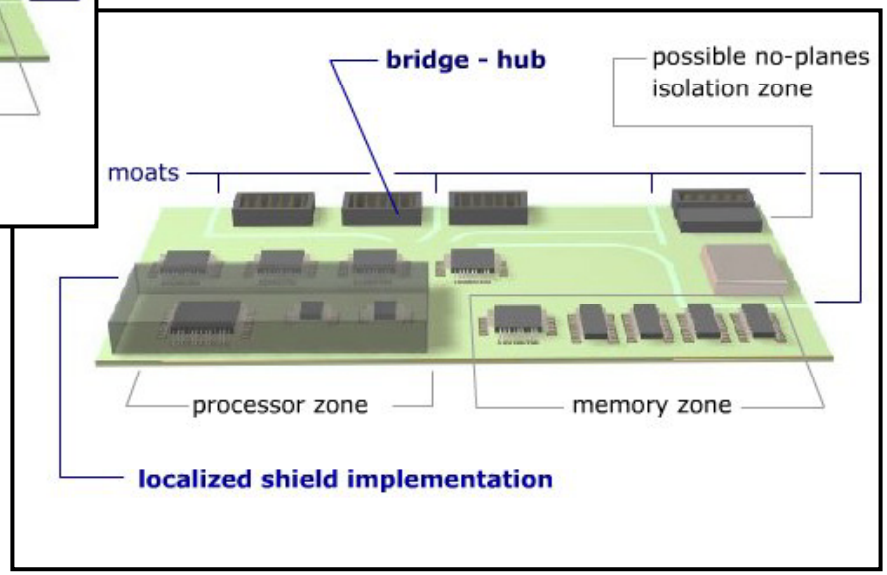
Implied Partitioning Topology of Circuit Board Without Chassis Plane





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Original “Recognition Plan” – Modified- Becomes “Summary”

→ **PARTITIONING** recognition plan is a subset part of the system-product “Common-mode Architecture”

→ “Common-mode Architecture” is a derivative of the system-product electrical / functional block architecture

→ System-product functionality is identified initially in “block” structures

→ “Block” structures set the pattern approach initially for X-Y Axes topology, followed by Z-Axis implementations for **PARTITIONING CONCEPTS**

→ Separation of High-Amplitude from Low-Amplitude (e.g. “sensitive” signals or circuit regions) for optimal functionality is a criteria set for **PARTITIONING**

→ Containment of specifically unique Spectral Regions **requires 3-Axes Views**

→ Protection of analogue circuits from digital spectra intrusions (S/N Ratios) and Exclusion of EMI Emission from interface – interconnecting cables **must include examination of field transfer involvements “through” chassis coupling**

→ Rejection of extraneously applied fields or currents (susceptibility-immunity factors) from functional intrusion will follow the partitioning concept in proportion to the approach.

Author Information:

W. Michael King is a systems design advisor who has been active in the development of over 1,000 system-product designs in a 44 year career. He serves an international client base as an independent advisor.
His full biography may be seen through his web site: www.SystemsEMC.com.

In addition to publishing original research on the subjects of the ESD dynamic waveform continuum and responses of cardiac pacemakers to electromagnetic fields, he has authored contributing articles to EDN Magazine, Oxford University CPD Newsletter, and Elliott Laboratories Compliance Advisory Service Newsletters as well as other publications.

Significantly, he is the author of *EMCT: High Speed Design Tutorial* (ISBN 0-7381-3340-X) which is the source of some of the graphics used in this presentation, and is available through Elliott Laboratories, co-branded with the IEEE Standards Information Network. As a tutorial, *EMCT* is the reference of presentation by Mr. King for his CPD course at Oxford University, England.